

John Paul S. Magbitang

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Education

Case Western Reserve University

Expected May 2028

Bachelor of Science in Electrical Engineering & Computer Engineering

Coursework: VLSI Design, Computer Architecture, Digital Systems Design, Digital Logic Laboratory, Logic Design and Organization, Embedded Systems Design and Laboratory, Electronic Circuits

Technical Skills

Languages: SystemVerilog, Verilog, C, C++, Python, RISC-V Assembly, Bash

RTL Design/Architecture: Pipelining, hazard detection/forwarding, static timing analysis, clock domain crossings

EDA: Xilinx Vivado, QuestaSim, Synopsys Design Compiler, Verilator, GTKWave, Yosys, OpenSTA, OpenLane

Software: VS Code, Git/GitHub, Docker, KiCAD, LTSpice, Siemens EDA (S-Edit, L-Edit & T-Spice), WSL

Hardware/Lab Equipment: Pynq Z2 FPGA (Zynq-7000), Raspberry Pi, Arduino Uno, Logic Analyzer, Oscilloscope, Digital Multimeter

Projects

5-Stage Pipelined RISC-V Processor (RV32IM)

August 2026

- Designed a 5-stage in-order RV32IM core in SystemVerilog featuring EX-stage branch resolution, full forwarding, load-use hazard detection and a 37-cycle iterative multiply/divide unit.
- Synthesized the core in SkyWater 130nm HD with Yosys and OpenSTA at 94 MHz pre-layout (0.088 mm², 8.7 mW); synthesized and implemented on a PYNQ-Z2 (Zynq-7020) FPGA at 92.7 MHz with on-board pass/fail reporting.
- Verified with self-checking benchmarks (CRC-32, Towers of Hanoi, bubble sort, FIR filter, matrix multiply) ranging from 0.67–0.75 IPC
- Currently integrating the core into an AXI4-Lite SoC with a custom bus master, a memory-mapped GPIO peripheral and a variable-latency RAM.

Asynchronous FIFO

September 2026

- Designed a parameterized dual-clock FIFO with Gray-coded pointers and 2FF synchronizers for clock-domain crossing; prevent overflow and underflow at any clock ratio
- Built a constrained-random, self-checking SystemVerilog testbench with a queue-based scoreboard and 6 checkers, randomizing clock ratios, traffic patterns, and data corner cases across 19 coverage goals

Experience

Embedded Systems Design Teaching Assistant

August 2026 – Present

Case School of Engineering

Cleveland, OH

- Support 40+ students in lab sessions every week in building and troubleshooting breadboard prototypes with the Raspberry Pi & Arduino Uno with sensors, LCDs, and other peripherals and help in debugging C, C++, & Python programs.
- Evaluate code demos and grade 15 lab reports every 2 weeks, returning written feedback for each report.

Control Systems Engineer Intern

May 2026 – August 2026

North Star BlueScope Steel

Delta, OH

- Built a thermal stereo camera acquisition system in C++ using OpenCV and Spinnaker SDK, generating calibrated 3D point clouds of steel coils to detect telescoping and defects which cost North Star roughly \$4,000 per coil in return processing alone.
- Automated file transfer and cleanup with 10 Bash scripts, moving slab telemetry data 24/7 over SFTP/FTP through data diodes for the plant's ongoing \$30M slab heating project installation.
- Developed an easy to use GUI in C++ in Qt for plant engineers for inspecting thermal images of 400+ coils a day.

Leadership & Activities

Founder & President | ASICWRU

March 2026 – Present

- Designed and taped out a single-cycle RISC-V processor (RV32I on GF180MCU) through Tiny Tapeout taking 1478 cells post-synthesis, verified zero setup violations across all PVT corners, and positive worst-case setup slack at slow corner.
- Authored an onboarding curriculum consisting of digital design concepts, explanation of open-source tools, and multiple onboarding projects including design & verification of an ALU, Synchronous FIFO, and a UART controller.
- Hosted biweekly workshops for 25+ active members and presentations on topics in the chip design domain including digital design fundamentals, Verilog/SystemVerilog, and industry relevant and open-source EDA tools.